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	Application No.	Applicant(s)	<u> </u>
Notice of Allowability			
	10/724,648 Examiner	FAZAN ET AL. Art Unit	
	Wai-Sing Louie	2814	
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.			
1. \boxtimes This communication is responsive to <u>2/3/05</u> .			
2. ☑ The allowed claim(s) is/are <u>28-64</u> .			
3. $igotimes$ The drawings filed on <u>01 December 2003</u> are accepted by	the Examiner.		
4.			
Attachment(s)			
1. X Notice of References Cited (PTO-892)	5. Notice of Informal P		D-152)
2. Notice of Draftperson's Patent Drawing Review (PTO-948)	 Interview Summary Paper No./Mail Date 		
 Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 3/8/05 			
4. Examiner's Comment Regarding Requirement for Deposit	8. Examiner's Stateme	ent of Reasons for Allo	wance
of Biological Material	9. 🗌 Other		

DETAILED ACTION

Allowable Subject Matter

The following is an examiner's statement of reasons for allowance:

The claimed invention is a semiconductor memory array comprising:

A plurality of memory cells arranged in a matrix of rows and columns, the plurality of memory cells include a first memory cell and a second memory cell, wherein the first and second memory cells each include at least a transistor to constitute the memory cell and wherein the transistor includes:

- A source region;
- A drain region;
- A body region disposed between the source region and the drain region, wherein the body region is electrically floating; and
- A gate spaced apart from, and capacitively coupled to, the body region; and wherein each memory cell includes:
 - o A first data state representative of a first charge in the body region; and
 - O A second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region; and wherein the source region of the transistor of the first memory cell and the source region of the transistor of the second memory cell are the same region.

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The prior art of record does not disclose or suggest either in singly or in combination the following limitations and other elements in the claims:

Reference Hu et al. (US 5,448,513) do not disclose the claimed operating states and removing charge from the body region.

Reference Kanamori (US 6,151,254) do not disclose the claimed operating states and removing charge from the body region.

Therefore, the above references do not disclose the claimed invention of present application and claims 28-64 are allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wai-Sing Louie whose telephone number is (571) 272-1709. The examiner can normally be reached on 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Wsl

March 11, 2005.

PRIVARY EXCAMPLE